2048x2048 HgCdTe FPA

August 1998

L.J. Kozlowski and K. Vural
Rockwell Science Center
Thousand Oaks, CA 91360

K. Hodapp
University of Hawaii
Institute for Astronomy
Honolulu, Hawaii 96822

W.E. Kleinhans
Valley Oak Semiconductor
Westlake Village, CA, 91362

ABSTRACT

Rockwell has begun developing infrared FPAs in the 2048^2 format. The first is the HAWAII-2, an infrared 2048^2 focal plane array (FPA) for next-generation infrared astronomy. It will supplant our HAWAII 1024^2 as the largest high-performance infrared imager available. As with our prior infrared FPAs, the flip-chip hybrid will consist of a low dark current, low-capacitance HgCdTe detector array mated to a low-noise CMOS silicon multiplexer via indium interconnects. The FPA's 18 µm pixel pitch accommodates both reasonable telescope optics and fabrication of the large, low-noise readout (≈40 x 40 mm^2) using world-class submicron CMOS.

1.0 INTRODUCTION

Infrared astronomy has benefited over the last decade from the availability of increasingly larger and more sensitive HgCdTe FPAs as shown in Figure 1. The first devices were 128x128 2.5µm FPAs developed for the Near Infrared Camera Multi-Object Spectrometer (NICMOS).[1] NICMOS1 and NICMOS2 comprised 16,384 pixels and 70,000 FETs. The next generation NICMOS, designated NICMOS3, was introduced in 1990 with 65,536 pixels and about 250,000 FETs. It also used 2.5µm HgCdTe detectors and multiplexers in 2µm CMOS to yield <40 e- read noise and dark current <0.1 e- at 78K.[2] High sensitivity hybrid infrared FPA technology leaped to the 1024x1024 format in 1994 with our HAWAII FPA. The HAWAII both increased the pixel count to over 1 million and the transistor count to over 3.4 million while also lowering the read noise to below 3 e- with Fowler sampling. In addition, a

1. K. Vural, L.J. Kozlowski and R.W. Rasche, "256 x 256 HgCdTe Focal Plane Array for the Hubble Space Telescope," *SPIE* **1320** (1990), pp.107-108.
2. D.E. Cooper, D. Q. Bui, R.B. Bailey, L.J. Kozlowski, and K. Vural, "Low-Noise Performance and Dark Current Measurements on the 256 x 256 NICMOS3 FPA," *SPIE* **1946** (1993) 170-178.

second 1024x1024 with capacitive transimpedance amplifier input developed in early 1995 raised the frame rate to about 24 Hz with 28 e- read noise. This device raised the transistor count to 4.3 million transistors.[3]

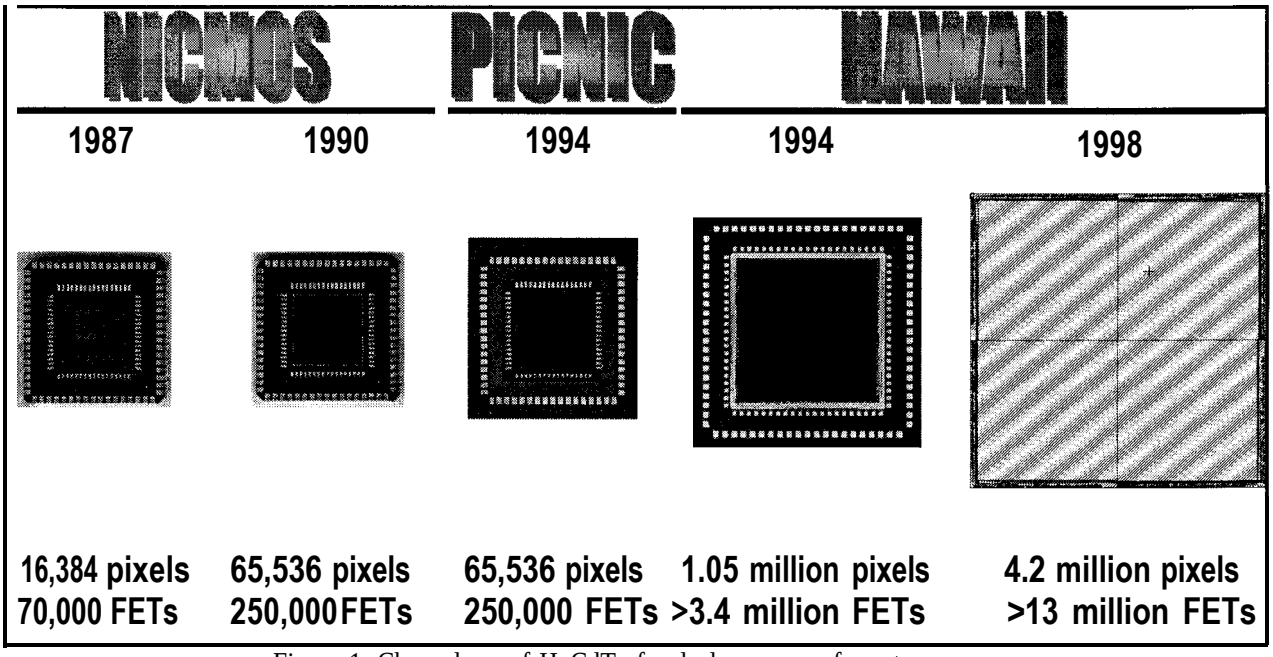

Figure 1. Chronology of HgCdTe focal plane arrays for astronomy.

In this paper we report our status in developing a 2.5um 2048x2048 HgCdTe FPA with source follower detector interface. Rockwell Science Center, the University of Hawaii, the European Southern Observatory and Subaru Telescope are jointly developing this device, which has 4.2 million pixels and ~13 million transistors. In Section 2 we describe the CMOS readout design. HgCdTe detector array design and fabrication are discussed in Section 3 for both our liquid phase and molecular beam epitaxial growth processes. We will fabricate, characterize and deliver the first IR hybrid FPAs in the final quarter of 1998, as discussed in Section 4.

2.0 HAWAII-2 2048x2048 CMOS READOUT

The design of the CMOS readout has been completed. The HAWAII-2 has four independent 1024x1024 quadrants. Ten CMOS-level clocks, two 5V power supplies (one analog and digital), one fixed dc bias and one variable dc bias are required for basic operation. Special design techniques have been used to minimize the electroluminescence[4] (i.e., self-glow which creates excess background signal and noise due to photon emission of hot carriers) of the various analog and digital circuits. Our goal is for the FPA dark current to be detector-limited at <0.01 electrons per second.

3. L. J. Kozlowski, K. Vural, D. E. Cooper, C.Y. Chen, D. M. Stephenson and S. A. Cabelli, "Low Noise, Low Power HgCdTe/Al_2O_3 1024x1024 FPAs," *SPIE* **2817** (1996), pp. 150-159.
4. S. Tam and C. Hu, "Hot-electron-induced photon and photocarrier generation in silicon MOSFET's," *IEEE Trans. Electron Devices,* **ED-31** (Sept. 1984) 1264-1273.

2.1. Readout Architecture and Fabrication Strategy

The 2048×2048 readout has four quadrants to facilitate its fabrication using standard submicron photolithography in conjunction with optical stitching. While wafer-scale photolithography can be used to fabricate wafer-scale devices having minimum features that are ≥1.5 µm, submicron features require wafer steppers having maximum field sizes of ~2 cm per side. The 1024×1024 HAWAII readout, for example, is the largest integrated circuit that can be conventionally fabricated using a GCA wafer stepper. Most available steppers have smaller fields; some newer steppers capable of supporting 0.25 µm processes have slightly larger fields. In any case, each 2048×2048 readout must therefore be lithographically composited using four optical fields to create each 4 cm × 4 cm circuit.

The fabrication alternative of employing wafer-scale photolithography is often problematic due to several largely intractable yield issues. First, such equipment is usually associated with older fabrication lines that are incapable of enabling the ultra-low defect densities necessary for fabricating large, high-quality readouts with zero defects. Second, the likelihood of poor yield is compounded by bloating the readout dimensions to support the larger minimum feature by increasing the pixel pitch. Unfortunately, yielding the much larger die further compounds the problem. Third, this type of lithography does not typically support wafers larger than 125 mm, so there are fewer die per wafer.

Figure 2 shows that we are populating each large-area 200 mm wafer with twelve 2048×2048 readouts. The figure also visually compares the size of a HAWAII-2 to the various field sizes for submicron wafer steppers manufactured by Canon, GCA and ASML.

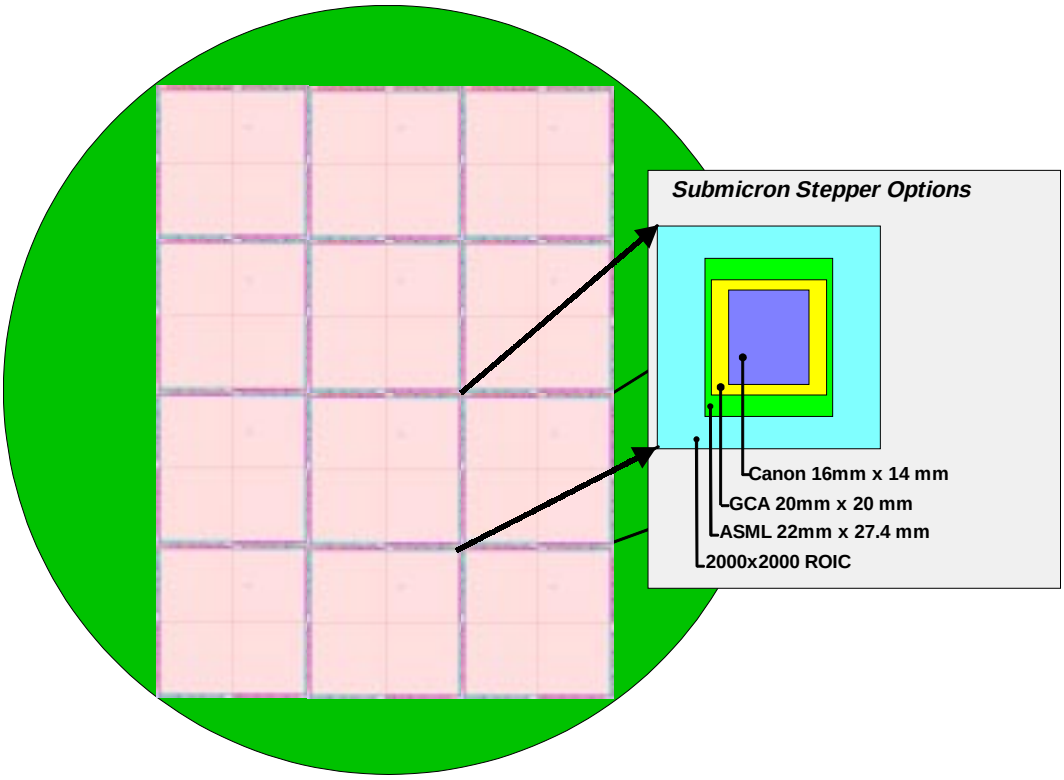

Figure 2. Each 200 mm wafer will have twelve 2048x2048 readouts.

Each readout is an array of MOSFET switches comprising cascaded source follower stages separated by MOSFET switches as shown in Figure 3. The signal voltage from each pixel in the array is read the

first stage source follower consisting of a pixel-based driver MOSFET and a current source FET shared among the 1024 elements in each column. The column bus output then drives the output source follower or can be read directly using external electronics to eliminate output amplifier glow. The various MOSFET switches are appropriately enabled and disabled to perform the functions of pixel access, reset and multiplexing. A maximum of eleven externally-supplied clocks will be required to facilitate an optional clocking mode which is provided to facilitate suppression of output amplifier nonuniformity. Since CMOS logic circuitry is used, the clock levels do not require precise adjustment for optimum performance. The architecture also maximizes fabrication yield.

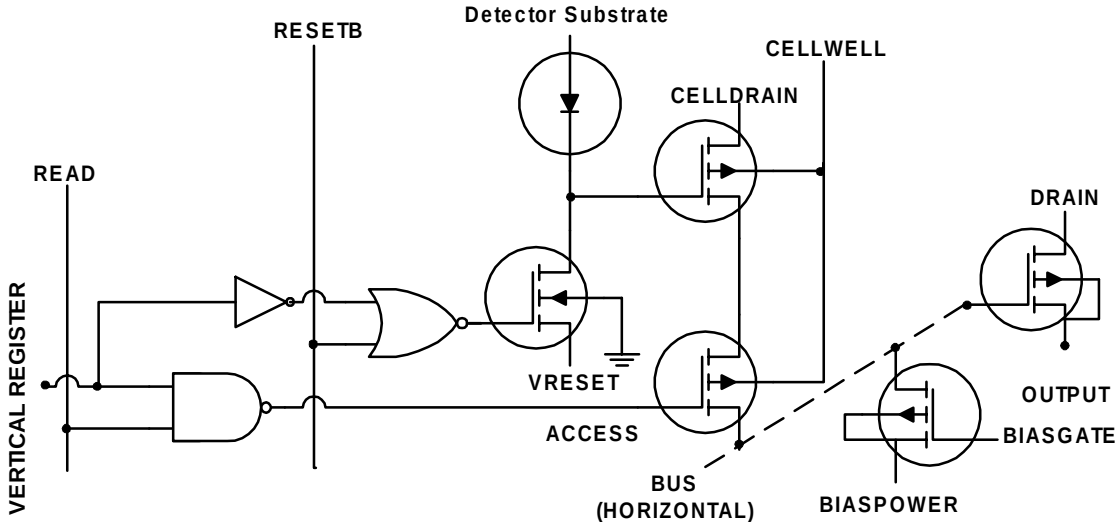

Figure 3. HAWAII-2: Key circuit elements including pixel and output buffer.

2.2. Detector Interface Circuit

The HAWAII-2 uses a source follower to read the photogenerated charge from each detector. This detector interface scheme works very well at low backgrounds, long frame times and applications where MOSFET glow must be negligible compared to the detector dark current. Photocurrent is stored directly on the detector capacitance. This requires the detector to be reverse-biased to maximize dynamic range. The detector voltage modulates the gate of a source follower whose drive FET is in the cell and whose current source is common to all the detectors in a column. The limited size of the cell transistor constrains its drive capability and thus the electrical bandwidth of the readout. The overall gain reduction through the readout's two source follower stages is expected to be ~0.8 under nominal bias at the maximum 2 MHz data rate. A charge-handling capacity of approximately 100,000 electrons is expected at 0.5V detector bias.

The source follower per detector circuit is capable of very low read noise when the detector capacitance is small and the concomitant photoconversion gain is high. Assuming that correlated double sampling is facilitated off-chip, the percentage of background-limited infrared performance (BLIP), η_{BLIP}, is approximately:

$$\eta_{BLIP} = \frac{\eta A_{\det} Q_B \tau_{\text{int}}}{\eta A_{\det} Q_B \tau_{\text{int}} + \frac{2kT\tau_{\text{int}}}{qR_{\det}} + N_{amp}^2 + \frac{2kT\tau_{\text{int}}}{qR_{rst}}}$$

where R_{rst} is the off resistance of the reset FET. The dominant read noise of the source follower is:[5]

$$N_{amp} \approx \frac{\sqrt{2}}{S_V}\left[\int_0^{\Delta f} V_n^2(f)\frac{1-\cos 2\pi f t}{\left[1+(2\pi f T_D)^2\right]}df\right]^{1/2}$$

where $V_n(f)$ is the MOSFET noise as a function of frequency, T_D is the correlated double sampler time constant given by $T_D=t/2$, Δf is the measurement bandwidth and S_v is the readout conversion gain in units of V/e-. If correlated multiple sampling techniques are not used, the read noise will instead be dominated by the kTC noise generated from resetting the total input capacitance comprising the detector, indium bump, and source follower gate.

Assuming that the HAWAII-2 multiplexer will have $V_n(f)$ of roughly 2 μV/Hz$^{1/2}$ at 1 Hz (i.e., the same as HAWAII), a 1 sec integration time, 34 fF capacitance, and external electronics noise of 35 μV rms, the predicted HAWAII-2 read noise is about 7.3 e- with CDS and 34 e- without. Figure 4 shows the predicted read noise vs. detector capacitance. Included are measured values and ranges for our 128×128, 256×256 and 1024×1024 FPAs[6] with source follower readout. The measured levels agree with the noise predicted for the nominal design values. Based on HAWAII results,[7] we expect that Fowler sampling will result in HAWAII-2 read noise <3 e-.

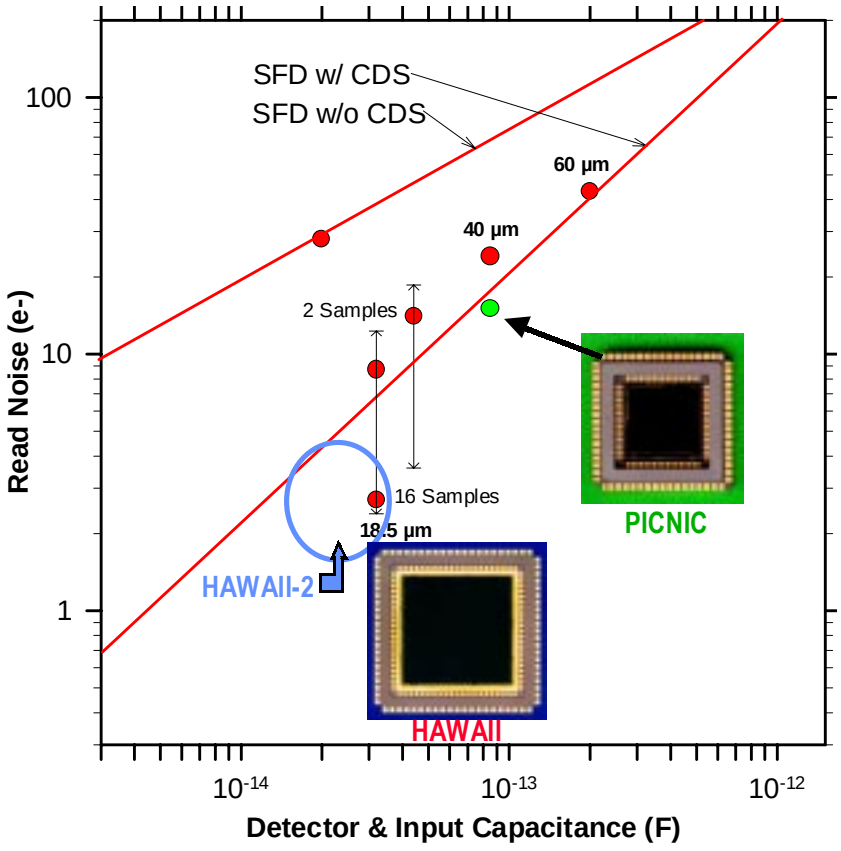

Figure 4. SFD FPA Read Noise: Predicted and Measured Values vs. Detector Capacitance.

5. J.R. Janesick, T.Elliott, S. Collins and H. Marsh, "The future scientific CCD," *SPIE* **501** (1984).
6. L.J. Kozlowski, K. Vural, S.C. Cabelli, A. Chen, D.E. Cooper, D.M. Stephenson and W.E. Kleinhans, "2.5μm PACE-I HgCdTe 1024x1024 FPA for Infrared Astronomy," *SPIE* **2268** (1994) 353-364.
7. G. Finger, European Southern Observatory, Private Communication.

2.3. Multiple Operating Modes

In addition to several subtle design refinements relative to the 1024x1024 readout, several optional operating modes have been added to the HAWAII-2 to increase flexibility and performance. The basic mode provides one output per quadrant for a total of four outputs per FPA and a maximum frame rate of about 2 Hz. A second mode provides eight outputs per quadrant for a total of 32 outputs per FPA. The additional outputs boost the maximum frame rate to ~16 Hz to facilitate higher background signal irradiance and use with detectors at longer cutoff wavelengths. Since the composition of HgCdTe can be appropriately tuned, 5 µm 2048^2 FPAs are hence feasible. The third mode also provides eight outputs per quadrant, but successively shuffles the video signals through each of the eight taps to suppress output amplifier offset nonuniformity. A fourth and final mode focuses on internal signal management; disabling this function operates the analog circuitry in a manner similar to the original HAWAII chip. Default operation, on the other hand, operates the device in a manner which should further lower the already low electrical crosstalk.

2.4. Expected Readout Characteristics

Table 1 lists the expected characteristics of the HAWAII-2. The key differences between it and the 1024x1024 HAWAII include:

- slight reduction in pitch from 18.5 µm to 18 µm
- increase in die size from 19.8 mm by 19.8 mm to ≈39 mm by 39 mm.
- change to zero-insertion-force (ZIF) pin grid array (PGA) package from leadless chip carrier
- change from four-output readout to programmable four- or 32-output readout with optional fixed pattern noise suppression mode
- compatibility with order-of-magnitude higher background irradiance
- reference output added to each quadrant to enable lower drift via differential signal processing
- default mode reduces electrical crosstalk

Table 1. HAWAII-2 Readout: Predicted Characteristics

Parameter	Minimum	Maximum	Units
Format	2048×2048		Pixels
Pixel Pitch	18		µm
Chip Package (Optional)	128 Pin		ZIF PGA
Die Size	≈39 x 39		mm^2
Input Circuit	Source Follower		
Temporal Noise Suppression	Off-chip: Correlated Double Sampling or Fowler Sampling		
Spatial Noise Suppression	8-Tap Video Averaging		
Supply Voltage	5		V
Integration Capacitance	20	35	10^{-15} F
Charge Capacity @0.5V	0.102	0.180	10^6 e-
Input Offset Nonuniformity		<5	mV p-p
Dynamic Range	>0.8	1	10^3
Output Taps	4	32	
Data Rate per Output Tap	1	≤2	MHz
Read Noise	<3	<9	e-
Conversion Gain (S_V)	≈3.5	≈7	µV/e-

Table 2 lists the clocks and biases needed to operate the FPA.

Table 2. HAWAII-2: CLOCKS AND BIASES

Input	Voltage (V)	Function
VDD, VDDA, CELLDRAIN, BIASPOWER	5	Power Supplies
VSS, MUXSUB	0V	Multiplexer Ground
O1	Clock	Mode Control
O2	Clock	Mode Control
DRAIN	5	Output Amp Supply/Bus Output Select
VRESET	0.5	Detector Reset Voltage
DSUB	0	Detector Common
BIASGATE	3.8	Sets SFD Current
VCLK	Clock	Fast Clock
LSYNC	Clock	Line Synchronization
CLK2	Clock	Line Clock 2
CLK1	Clock	Line Clock 1
CLKB2	Clock	Line Clock Bar 2
CLKB1	Clock	Line Clock Bar 1
FSYNC	Clock	Frame Synchronization
RESET	Clock	Pixel Reset Clock
READ	Clock	Pixel Read Clock
LRST	Clock	Output Shuffle Reset

3.0 HgCdTe DETECTOR ARRAYS

Rockwell has emphasized photovoltaic HgCdTe because its material properties for application to infrared detectors are fundamentally superior to those of other intrinsic materials such as indium antimonide (InSb), and competing extrinsic detectors including doped silicon, quantum well GaAs and PtSi.[8] Though this ternary system has posed numerous producibility challenges over two decades of development, we now produce HgCdTe arrays with near-theoretical characteristics and adequate uniformity at cutoff wavelengths from ~1.5 µm to >16 µm via molecular beam epitaxy (MBE). We use liquid phase epitaxy (LPE) to produce SWIR and MWIR FPAs with >99.9% and >99% pixel operability, respectively.

The junctions are formed by ion implantation in both cases. However, the detector architectures are significantly different between the LPE and MBE approaches; the former is an *n*-on-*p* process incorporating homojunction formation in vacancy-doped base material using boron ion implantation. The latter is a *p*-on-*n* heterostructure process incorporating As implantation through a wider bandgap capping layer into In-doped base material. The resulting double layer planar heterostructure (DLPH) MBE layers are grown on <211> CdZnTe substrates; this results in much lower defect densities (mid-10^4 to low-10^5 range) than LPE material which is grown on <111> lattice-mismatched substrates (low-10^6 range). The CdZnTe substrates are smaller (~4x4 and 4x6 cm^2 are common) than the sapphire LPE substrates.

We are fabricating 2.5 µm 2048x2048 FPAs using detector arrays via our standard (LPE) and highest performance (MBE) detector growth technologies. The latter focal plane arrays are expected to provide enhanced science because these FPAs will have:

8. A. Rogalski and J. Piotrowski, "Intrinsic Infrared Detectors," Progress in Quantum Electronics, Pergamon Press, 12(2/3), (1988)

- much lower dark current
- enhanced uniformity of key characteristics including breakdown voltage and 1/f noise
- negligible persistence

The higher performance material is also allowing extension of cutoff wavelength to the MWIR regime while enhancing device performance relative to the smaller InSb-based arrays that are currently available.

The performance benefits of the DLPH MBE HgCdTe detector technology are best shown by the dark current density data in Figure 5, a plot of dark current density, J_{dark}, vs. operating temperature. The figure contains typical InSb data[9] for direct comparison with the HgCdTe alternatives, representative PACE HgCdTe arrays at ~5 µm and 2.5 µm, and DLPH MBE HgCdTe arrays at 5.2 µm and 2.2 µm. The MBE-based dark current densities are superior to PACE and in good agreement with the theoretical limit for conventional (unthinned) p/n detectors in any material. Detector dark current relative to PACE at a specific operating temperature is reduced by nearly two orders of magnitude at 5 µm and several orders of magnitude at 2.5 µm. The key issue is the extent to which the total pixel yield will be limited by the quantity of pixels degraded by various defect-related mechanisms rather than fundamental considerations.

4.0 IR FPA PERFORMANCE

The first HAWAII-2 FPAs will be fabricated as soon as the multiplexers are available. We anticipate that these will perform similarly to the existing HAWAII FPA because the key design features are essentially identical. The HAWAII 1024×1024 is the largest high sensitivity IR FPA currently available. Data taken at zero background at 78K and 66K typically show upper limits on dark current of 0.08 e-/s and 0.04 e-/s, respectively. HAWAII read noise is typically <9 e- using conventional correlated double sampling (CDS). Fowler signal measurement techniques have yielded read noise <3 e-.

9. J.D. Vincent, Fundamentals of Infrared Detector Operation and Testing, Wiley (1990)

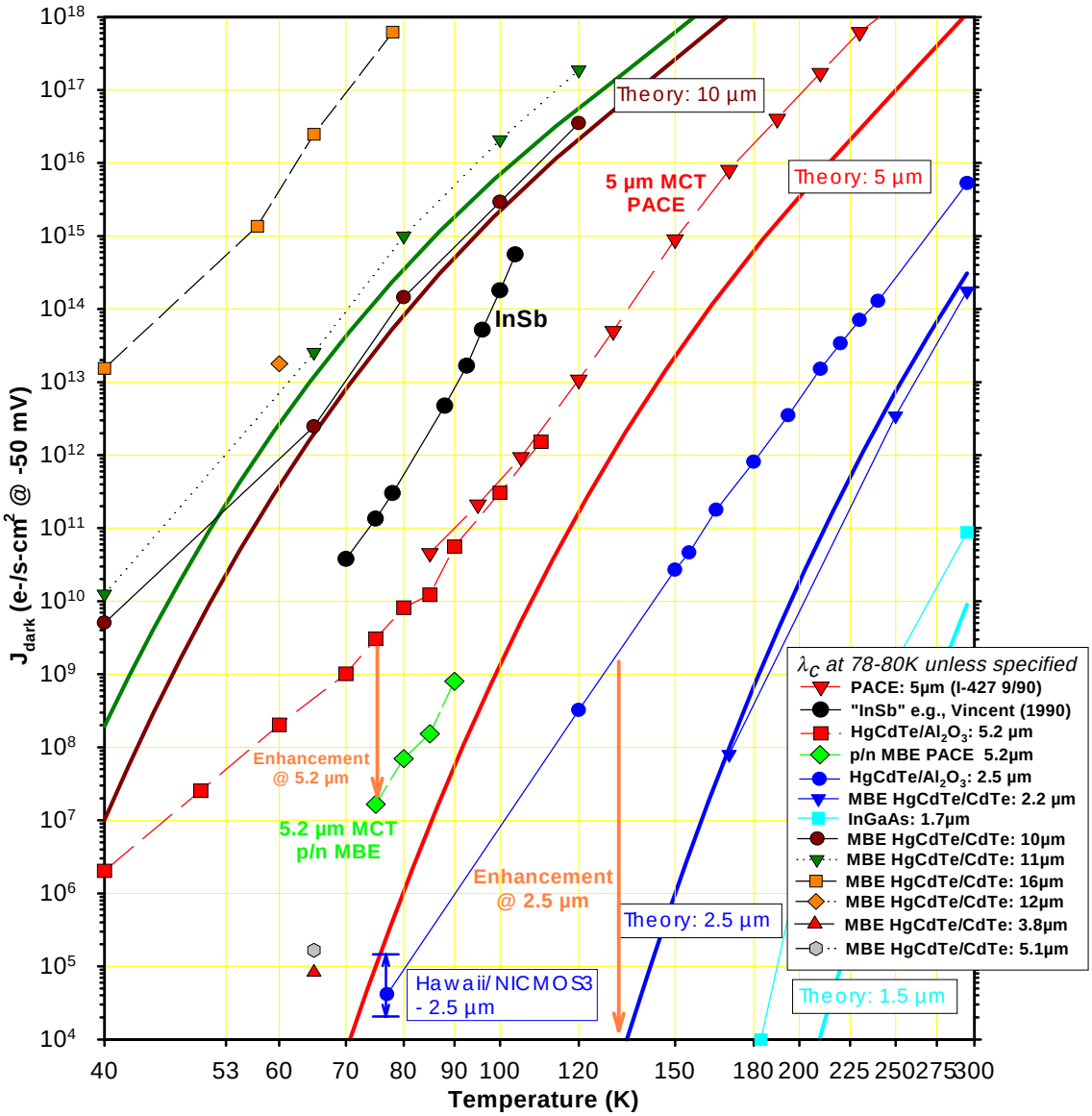

Figure 5. Performance advantages of DLPH MBE HgCdTe.

5. CONCLUSION

The HAWAII-2 FPA is being developed using design and fabrication methodologies that should maximize the probability of success for this ambitious effort. We anticipate excellent performance characteristics including ≈4.2 million pixels, ≤3 e- read noise, mean dark current <0.1 e-/s at 78K, high broadband quantum efficiency (>50% from 1.0 to 2.5 µm), and negligible persistence using MBE-grown detector arrays. In addition, the HAWAII-2 is exploiting several lessons learned from the HAWAII and will thus offer key enhancements to improve the science that can be performed using these arrays including, possibly, extension of spectral coverage to 5 µm.